

Features

- Peripheral component interconnect (PCI) standard form factor expansion card
- Supports in-circuit reconfiguration with an EPC1 Configuration EPROM, or the BitBlaster™, ByteBlaster™, or ByteBlasterMV™ download cable
- Includes an EPF10K30RC240-3 device
- 128 KBytes of on-board SRAM upgradable to 256 KBytes
- Local-side function can interface to a standard parallel port or a standard VGA port
- I/O headers allowing users to interface with extra prototype devices
- External power connection for stand alone operation
- On-board headers
 - Connect to either the BitBlaster or the ByteBlaster download cable for device configuration
 - Allow fast external local-side clock input

General Description

The PCI prototype board is designed to work with the `pci_a` MegaCore™ function and is for demonstration purposes only. This data sheet provides signal connections, jumper settings, supported components, and board options for the Altera PCI prototype board, version 1.0.

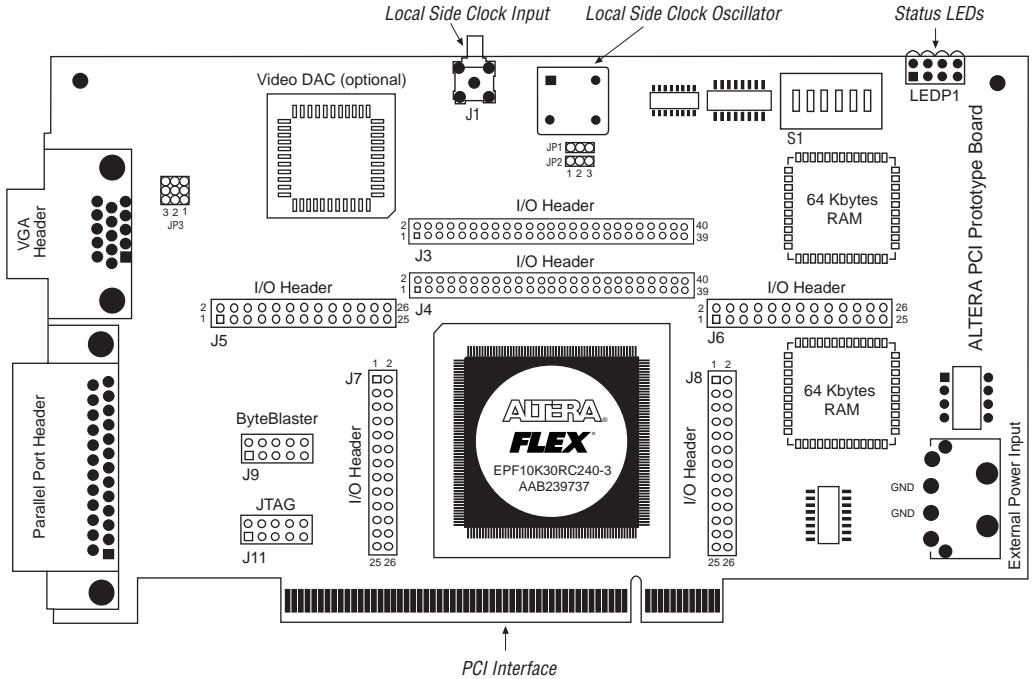


For installation instructions, refer to “Getting Started with the `pci_a` Prototype Board” in the `readme.htm` file included with the `pci_a` function.

Functional Description

Figure 1 shows the PCI prototype board block diagram.

Figure 1. PCI Prototype Board Block Diagram



Signal Connections

Signals pass through the PCI prototype board via the PCI interface or external sources and connect to various board components. To view up-to-date PCI prototype board schematics, refer to the Altera FTP site at <ftp.altera.com/pub/megacore/pci/board/>. Table 1 defines the schematic references, and Table 2 lists the board connections illustrated in the schematics.

Table 1. Schematic Reference Definitions (Part 1 of 2)

Reference	Definition
P1.A<n> or P1.B<n>	P1 = PCI interface; A = front of board; B = back of board; <n> = pin number
U8.<n>	U8 = EPF10K30; <n> = pin number
J<hn>.<n>	J = header; <hn> = header number; <n> = pin number
JP<jn>.<n>	JP = jumper; <jn> = jumper number; <n> = pin number
D<dn>.<n>	D = diode; <dn> = diode number; <n> = pin number
R<m>.<n>	R = resistor; <m> = resistor number; <n> = pin number
U3.<n>	U3 = video DAC device; <n> = pin number

Table 1. Schematic Reference Definitions (Part 2 of 2)

Reference	Definition
C<dn>.<n>	C = capacitor; <dn> = diode number; <n> = pin number
LEDP1	LEDP1 = light emitting diode
RP<rpn>.<n>	RP = resistor package; <rpn> = resistor package number; <n> = pin number
U2.<n>	U2 = 7404; <n> = pin number
S1.<n>	Configuration dipswitches; <n> = pin number
U6.<n>	EPC1; <n> = pin number
U1.<n>	Clock device; <n> = pin number
U4.<n>	Cache memory; <n> = pin number
U7.<n>	Cache memory; <n> = pin number

Table 2 shows the sequence of PCI prototype board connections, e.g., signal ad0 connects through pin 58 of the PCI interface to pin 120 of the EPF10K30 device.

Table 2. PCI Prototype Board Connections (Part 1 of 7) Note (1)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
AD0	P1.A58	U8.120	–	–	–	–
AD1	P1.B58	U8.119	–	–	–	–
AD2	P1.A57	U8.118	–	–	–	–
AD3	P1.B56	U8.115	–	–	–	–
AD4	P1.A55	U8.114	–	–	–	–
AD5	P1.B55	U8.113	–	–	–	–
AD6	P1.A54	U8.111	–	–	–	–
AD7	P1.B53	U8.110	–	–	–	–
AD8	P1.B52	U8.109	–	–	–	–
AD9	P1.A49	U8.108	–	–	–	–
AD10	P1.B48	U8.107	–	–	–	–
AD11	P1.A47	U8.106	–	–	–	–
AD12	P1.B47	U8.105	–	–	–	–
AD13	P1.A46	U8.103	–	–	–	–
AD14	P1.B45	U8.102	–	–	–	–
AD15	P1.A44	U8.101	–	–	–	–
AD16	P1.A32	U8.100	–	–	–	–
AD17	P1.B32	U8.99	–	–	–	–
AD18	P1.A31	U8.88	–	–	–	–
AD19	P1.B30	U8.87	–	–	–	–
AD20	P1.A29	U8.86	–	–	–	–

Table 2. PCI Prototype Board Connections (Part 2 of 7) *Note (1)*

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
AD21	P1.B29	U8.84	–	–	–	–
AD22	P1.A28	U8.83	–	–	–	–
AD23	P1.B27	U8.82	–	–	–	–
AD24	P1.A25	U8.79	–	–	–	–
AD25	P1.B24	U8.78	–	–	–	–
AD26	P1.A23	U8.76	–	–	–	–
AD27	P1.B23	U8.72	–	–	–	–
AD28	P1.A22	U8.71	–	–	–	–
AD29	P1.B21	U8.70	–	–	–	–
AD30	P1.A20	U8.68	–	–	–	–
AD31	P1.B20	U8.67	–	–	–	–
blue-5	J2.3	JP3.8	–	–	–	–
btblue-5	D1.3	U3.37	JP3.9	R5.1	–	–
btclk-5	R2.2	JP2.2	U3.18	R1.1	–	–
btfsadj-5	R11.1	U3.36	–	–	–	–
btgreen	U3.38	D2.3	JP3.6	R6.1	–	–
btred-5	D3.3	U3.39	JP3.3	R7.1	–	–
btvref-5	U3.35	C7.1	–	–	–	–
C/BE/0	P1.A52	U8.117	–	–	–	–
C/BE/1	P1.B44	U8.116	–	–	–	–
C/BE/2	P1.B33	U8.66	–	–	–	–
C/BE/3	P1.B26	U8.65	–	–	–	–
CLK	P1.B16	U8.211	–	–	–	–
CONF_DONE	U8.2	J9.3	U2.9	–	–	–
conf_doneled	LEDP1.3	U2.8	–	–	–	–
config/	U8.121	RP2.6	J9.5	–	–	–
confsou	U2.3	RP1.2	S1.12	U2.1	–	–
DATA0	U8.180	RP2.8	J9.9	U6.1	–	–
DCLK	U8.179	J9.1	U6.2	–	–	–
DEVSEL/	P1.B37	U8.80	–	–	–	–
GNT/	P1.A17	U8.55	–	–	–	–
green-5	J2.2	JP3.5	–	–	–	–
IDSEL	P1.A26	U8.64	–	–	–	–
IRDY	P1.B35	U8.74	–	–	–	–
inta	U8.54	P1.A6	–	–	–	–
lclk	U8.91	R10.1	R18.2	R15.1	–	–
lclkb-5	R9.1	JP2.3	–	–	–	–

Table 2. PCI Prototype Board Connections (Part 3 of 7) Note (1)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
LOCK/	P1.B39	U8.94	–	–	–	–
MSEL0	U8.124	RP2.9	R19.1	–	–	–
MSEL1	U8.123	RP2.10	R16.1	–	–	–
N00002	U8.178	RP2.2	–	–	–	–
N00003	U8.3	RP2.1	–	–	–	–
N00004	U8.59	RP2.3	–	–	–	–
N00008	R8.1	C5.2	–	–	–	–
N00009	U3.34	R8.2	–	–	–	–
N00017	JP1.1	J1.CENTER	–	–	–	–
N00018	JP1.2	R9.2	R10.2	–	–	–
N00019	U1.3	JP1.3	–	–	–	–
N00020	U1.1	RP1.7	–	–	–	–
N00021	RP1.8	U4.20	–	–	–	–
N00022	RP1.9	U4.46	–	–	–	–
N00023	RP1.10	U7.20	–	–	–	–
N00024	RP1.11	U7.46	–	–	–	–
PAR	P1.A43	U8.98	–	–	–	–
PERR/	P1.B40	U8.95	–	–	–	–
p1d1	U8.6	J5.23	U3.40	–	–	–
p1d2	U8.7	J5.24	U3.41	–	–	–
p1d3	U8.8	J5.21	U3.42	–	–	–
p1d4	U8.9	J5.22	U3.43	–	–	–
p1d5	U8.11	J5.19	U3.44	–	–	–
p1d6	U8.12	J5.20	U3.1	–	–	–
p1d7	U8.13	J5.17	U3.2	–	–	–
p1d8	U8.14	J5.18	U3.3	–	–	–
p1d9	U8.15	J5.15	R14.2	JP3.7	D6.1	–
p1d10	U8.17	J5.16	R13.2	JP3.4	D5.1	–
p1d11	U8.18	J5.13	R12.2	JP3.1	D4.1	–
p1d12	U8.19	J10.13	J5.14	–	–	–
p1d13	U8.20	J10.12	J5.11	–	–	–
p1d14	U8.21	J10.11	J5.12	–	–	–
p1d15	U8.23	J10.10	J5.9	–	–	–
p1d16	U8.24	J10.9	J5.10	–	–	–
p1d17	U8.25	J10.8	J5.7	–	–	–
p1d18	U8.26	J10.7	J5.8	–	–	–
p1d19	U8.28	J10.6	J5.5	–	–	–

Table 2. PCI Prototype Board Connections (Part 4 of 7) *Note (1)*

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
p1d20	U8.29	J10.5	J5.6	–	–	–
p1d21	U8.30	J10.17	J5.3	–	–	–
p1d22	U8.31	J10.4	J5.4	–	–	–
p1d23	U8.33	J10.16	J7.3	–	–	–
p1d24	U8.34	J10.3	J7.4	–	–	–
p1d25	U8.35	J10.15	J7.5	–	–	–
p1d26	U8.36	J10.2	J7.6	–	–	–
p1d27	U8.38	J10.14	J7.7	–	–	–
p1d28	U8.39	J10.1	J7.8	–	–	–
p1d29	U8.40	J7.9	S1.10	RP1.3	–	–
p1d30	U8.41	J7.10	S1.9	RP1.4	–	–
p1d31	U8.43	J7.11	S1.8	RP1.5	–	–
p1d32	U8.44	J7.12	S1.7	RP1.6	–	–
p1d33	U8.45	J7.13	–	–	–	–
p1d34	U8.46	J7.14	–	–	–	–
p1d35	U8.48	J7.15	–	–	–	–
p1d36	U8.49	J7.16	–	–	–	–
p1d37	U8.50	J7.17	–	–	–	–
p1d38	U8.51	J7.18	–	–	–	–
p1d39	U8.53	J7.19	–	–	–	–
p1d40	U8.61	J7.20	–	–	–	–
p1d41	U8.62	J7.21	–	–	–	–
p1d42	U8.63	J7.22	–	–	–	–
p1d43	J7.23	–	–	–	–	–
p1d44	U8.126	J7.24	–	–	–	–
p1d45	U8.127	J8.24	U7.51	R4.2	U4.51	R3.1
p1d46	U8.128	J8.23	U7.50	U4.50	–	–
p1d47	U8.129	J8.22	U7.5	U4.5	–	–
p1d48	U8.131	J8.21	U7.2	U4.2	–	–
p1d49	U8.132	J8.20	U7.1	U4.1	–	–
p1d50	U8.133	J8.19	U7.52	U4.52	–	–
p1d51	U8.134	J8.18	U7.3	–	–	–
p1d52	U8.136	J8.17	U7.4	–	–	–
p1d53	U8.137	J8.16	U4.3	–	–	–
p1d54	U8.138	J8.15	U4.4	–	–	–
p1d55	U8.139	J8.12	U7.34	–	–	–
p1d56	U8.141	J8.11	U7.35	–	–	–

Table 2. PCI Prototype Board Connections (Part 5 of 7) *Note (1)*

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
p1d57	U8.142	J8.10	U7.38	–	–	–
p1d58	U8.143	J8.9	U7.39	–	–	–
p1d59	U8.144	J8.8	U7.40	–	–	–
p1d60	U8.146	J8.7	U7.41	–	–	–
p1d61	U8.147	J8.6	U7.44	–	–	–
p1d62	U8.148	J8.5	U7.45	–	–	–
p1d63	U8.149	J8.4	U7.8	–	–	–
p1d64	U8.151	J8.3	U7.9	–	–	–
p1d65	U8.152	J6.24	U7.12	–	–	–
p1d66	U8.153	J6.23	U7.13	–	–	–
p1d67	U8.154	J6.22	U7.14	–	–	–
p1d68	U8.156	J6.21	U7.15	–	–	–
p1d69	U8.157	J6.20	U7.18	–	–	–
p1d70	U8.158	J6.19	U7.19	–	–	–
p1d71	U8.159	J6.18	U4.34	–	–	–
p1d72	U8.161	J6.17	U4.35	–	–	–
p1d73	U8.162	J6.16	U4.38	–	–	–
p1d74	U8.163	J6.15	U4.39	–	–	–
p1d75	U8.164	J6.12	U4.40	–	–	–
p1d76	U8.166	J6.11	U4.41	–	–	–
p1d77	U8.167	J6.10	U4.4	–	–	–
p1d78	U8.168	J6.9	U4.45	–	–	–
p1d79	U8.169	J6.8	U4.8	–	–	–
p1d80	U8.171	J6.7	U4.9	–	–	–
p1d81	U8.172	J6.6	U4.12	–	–	–
p1d82	U8.173	J6.5	U4.13	–	–	–
p1d83	U8.174	J6.4	U4.14	–	–	–
p1d84	U8.175	J6.3	U4.15	–	–	–
p1d85	U8.181	J4.33	U4.18	–	–	–
p1d86	U8.182	J4.34	U4.19	–	–	–
p1d87	U8.183	J3.33	U7.26	U4.26	–	–
p1d88	U8.184	J3.34	U7.25	U4.25	–	–
p1d89	U8.185	J4.31	U7.24	U4.24	–	–
p1d90	U8.186	J4.32	U7.23	U4.23	–	–
p1d91	U8.187	J3.31	U7.22	U4.22	–	–
p1d92	U8.188	J3.32	U7.21	U4.21	–	–
p1d93	U8.190	J4.29	U7.7	U4.7	–	–

Table 2. PCI Prototype Board Connections (Part 6 of 7) Note (1)

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
p1d94	U8.191	J4.30	U7.6	U4.6	–	–
p1d95	U8.192	J3.29	U7.49	U4.49	–	–
p1d96	U8.193	J3.30	U7.48	U4.48	–	–
p1d97	U8.194	J4.25	U7.47	U4.47	–	–
p1d98	U8.195	J4.26	U7.33	U4.33	–	–
p1d99	U8.196	J3.25	U7.32	U4.32	–	–
p1d100	U8.198	J3.26	U7.31	U4.31	–	–
p1d101	U8.199	J4.23	U7.30	U4.30	–	–
p1d102	U8.200	J4.24	U7.29	U4.29	–	–
p1d103	U8.201	J3.23	–	–	–	–
p1d104	U8.202	J3.24	U3.19	–	–	–
p1d105	U8.203	J4.21	U3.20	–	–	–
p1d106	U8.204	J4.22	U3.21	–	–	–
p1d107	U8.206	J3.21	U3.22	–	–	–
p1d108	U8.207	J3.22	U3.23	–	–	–
p1d109	U8.208	J4.19	U3.24	–	–	–
p1d110	U8.209	J4.20	U3.25	–	–	–
p1d111	U8.213	J3.19	U3.26	–	–	–
p1d112	U8.214	J3.20	U3.8	–	–	–
p1d113	U8.215	J4.17	U3.9	–	–	–
p1d114	U8.217	J4.18	U3.10	–	–	–
p1d115	U8.218	J3.17	U3.11	–	–	–
p1d116	U8.219	J3.18	U3.12	–	–	–
p1d117	U8.220	J4.13	U3.13	–	–	–
p1d118	U8.221	J4.14	U3.14	–	–	–
p1d119	U8.222	J3.13	U3.15	–	–	–
p1d120	U8.223	J3.14	–	–	–	–
p1d121	U8.225	J4.11	–	–	–	–
p1d122	U8.226	J4.12	–	–	–	–
p1d123	U8.227	J3.11	–	–	–	–
p1d124	U8.228	J3.12	–	–	–	–
p1d125	U8.229	J4.9	–	–	–	–
p1d126	U8.230	J4.10	–	–	–	–
p1d127	U8.231	J3.9	–	–	–	–
p1d128	U8.233	J3.10	JP2.1	–	–	–
p1d129	U8.234	J4.7	U3.7	–	–	–
p1d130	U8.235	J4.8	U3.6	–	–	–

Table 2. PCI Prototype Board Connections (Part 7 of 7) *Note (1)*

Signal	Connection 1	Connection 2	Connection 3	Connection 4	Connection 5	Connection 6
p1d131	U8.236	J3.7	–	–	–	–
p1d132	U8.237	J3.8	–	–	–	–
p1d133	U8.238	J4.5	–	–	–	–
p1d134	U8.239	J4.6	J2.14	–	–	–
p1d135	U8.240	J3.5	J2.13	–	–	–
red-5	J2.1	JP3.2	–	–	–	–
REQ/	P1.B18	U8.56	–	–	–	–
req64/-2	R17.2	P1.A60	–	–	–	–
RST/	P1.A15	U8.210	–	–	–	–
selbitbl/	LEDP1.2	U2.6	–	–	–	–
selepc/-7	LEDP1.1	U2.4	–	–	–	–
SERR/	P1.B42	U8.97	–	–	–	–
spare-7	RP1.1	S1.11	–	–	–	–
status/	U8.60	RP2.7	J9.7	U6.3	–	–
STOP/	P1.A38	U8.81	U8.212	–	–	–
tclk	U8.1	P1.B2	J11.1	–	–	–

Note:

(1) Altera-reserved signal names are shown in upper case Courier type.

Jumper Settings

Table 3 lists default jumper settings and describes optional pin connections for the stopn, trdyn, and framen bidirectional signals.

Table 3. Jumper Settings (Part 1 of 2)

Item	Default Setting	Schematic Reference, <i>Note (1)</i>	Description
JP3	A-B	Video digital analog converter (DAC)	The board is shipped without the Brooktree Bt121 video DAC, and the three jumpers (one for each color channel) are set to the A-B position. This configuration allows the EPF10K30 device to drive the VGA outputs directly, for a total of 8 colors. To configure the board for use with the Bt121 video DAC, set the JP3 jumpers to the B-C position.

Table 3. Jumper Settings (Part 2 of 2)

Item	Default Setting	Schematic Reference, <i>Note (1)</i>	Description
JP4	1-2	FLEX® 10K PCI controller	In the <code>pci_a</code> function, the bidirectional signal <code>stopn</code> is split into two separate input and output pins (212, 81). To configure the board to use the <code>stopn</code> signal driven by one bidirectional pin (81), set JP4 to 2-3. JP4 is a solder jumper on the bottom side of the board.
JP5	1-2	FLEX 10K PCI controller	In the <code>pci_a</code> function, the bidirectional signal <code>trdyn</code> is split into two separate input and output pins (90, 75). To configure the board to use the <code>trdyn</code> signal driven by one bidirectional pin (75), set JP5 to 2-3. JP5 is a solder jumper on the bottom side of the board.
JP6	1-2	FLEX 10K PCI controller	In the <code>pci_a</code> function, the bidirectional signal <code>framen</code> is split into two separate input and output pins (92, 73). To configure the board to use the <code>framen</code> signal driven by one bidirectional pin (73), set JP6 to 2-3. JP6 is a solder jumper on the bottom side of the board.
S1	–	Configuration logic and Joint Test Action Group (JTAG) interface	S1 is not needed for device configuration. However, bits 3 through 6 are connected to the EPF10K30 I/O pins and can be used as desired.

Note:

- (1) Refer to the Altera FTP site for up-to-date PCI prototype board schematics at <ftp.altera.com/pub/megacore/pci/board/>.

Supported Components

Table 4 lists all components supported by the PCI prototype board; however, not all components are shipped with the board. See "[Board Options](#)" on page 12 for more information.

Table 4. Supported Components (Part 1 of 2)

Component	Manufacturer Part Number	Quantity	Schematic Reference <i>Note (1)</i>
0.01UF, 0805	NOVACAP 0805Z103M500N	6	C1, C5, C6, C8, C17, C23
0.1UF, 0805	NOVACAP 0805Z104M500	32	C2, C3, C7, C10, C12, C13, C14, C15, C16, C18, C19, C20, C21, C22, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C42, C44, C45
10UF, 6032	Matsuo 267M1602106K-720	7	C4, C9, C11, C24, C40, C41
DA204, SOT-23	ROHM DA204	3	D1, D2, D3, D4, D5, D6
JUMP 3, HEADER 3 x 1	Samtec TSW-103-07-G-S	2	JP1, JP2
HEADER 3 x 3	Samtec TSW-103-07-G-T	1	JP3

Table 4. Supported Components (Part 2 of 2)

Component	Manufacturer Part Number	Quantity	Schematic Reference <i>Note (1)</i>
SMB-BNC, SMB-RT	AMP 413996-2	1	J1
DB15F MINI	AMP 748390-5	1	J2
HEADER 20 x 2	Samtec TSW-120-07-G-D	2	J4, J3
HEADER 13 x 2	Samtec TSW-113-07-G-D	4	J5, J6, J7, J8
HEADER 5 x 2	Samtec TSW-105-07-G-D	2	J11, J9
CONNECTOR DB25, DB25 FEMALE	Generic	1	J10
PWR CON4 RT ANGLE	Molex 15-24-4041	1	J12
LED-QUAD4, LED- QUAD4	Dialight 555-4003	1	LEDP1
10KRP, SOMC16	Dale SOMC-1601-103K	2	RP2, RP1
240 1/10W 5%, 0805	ROHM MCR10JW241	6	R1, R2, R3, R4, R15, R18
75.0 1/10W 1%, 0805	ROHM MCR10FW7501	3	R5, R6, R7
15 1/10W 5%, 0805	ROHM MCR10JW150	1	R8
10 1/10W 5%, 0805	ROHM MCR10JW100	2	R9, R10
143 1/10W 1%, 0805	ROHM MCR10FW1432	1	R11
10K 1/10W 5%, 0805	ROHM MCR10JW103	4	R12, R13, R14, R17
0, 0805	ROHM MCR10JW000	2	R16, R19
SW DIP-6, DIPSW12	Grayhill 76PSB06	1	S1
50 MHz, SG-531	EPSON SG-531PH-50.000MC	1	U1
74HCT04, S014	TI SN74HCT04D	1	U2
BT121KPJ50, PLCC44	Brooktree BT121KPJ50	1	U3
CY7C1032-8JC, PLCC52	Cypress CY7C1032-8JC	2	U7, U4
T-FILTER, NFM61R	Murata NFM61R30T472	0	U5
EPC1, DIP8	Altera EPC1PC8	1	U6
EPF10K30, RQFP240	Altera EPF10K30RC240-3	1	U8
SOCKET, QFP240	Altera PL-SKT/Q240	1	XU2
SOCKET, PLCC44	AMP 821979-3	1	XU3
SOCKET, DIP8	AMP 2-641260-1	1	XU9

Note:

- (1) Refer to the Altera FTP site for up-to-date PCI prototype board schematics at [ftp.altera.com/pub/megacore/pci/board/](ftp://altera.com/pub/megacore/pci/board/).

Board Options

The PCI prototype board schematics illustrate optional items and configuration modes. Tables 5 through 8 list video DAC, clock device, SRAM, and configuration options for the board.

Table 5. Video DAC Options

Board Setup	Brooktree BT121KPJ50	R8, R7, R6, R5, R2, R1, R11	C40, C23, C4, C17, C1, C8, C6, C5, C7	T-Filter	JP2
FLEX 10K device drives monitor, <i>Note (1)</i>	Removed	Removed	Removed	Removed	Removed
Video DAC drives monitor	Mount	Mount	Mount	Mount	Mount

Table 6. Clock Device Options

Option	Part Number	Resistors	Description
User-defined clock device, <i>Note (1)</i>	–	–	Other frequencies
Suggested clock device	EPSON SG-531PH-50.000MC	R9, R10, R19, R15	Suggested 50-MHz clock device
On-board clock device, <i>Notes (1), (2)</i>	Removed	Removed	Default

Table 7. SRAM Options

Part Number	Memory Size (System Cache Memory)	Maximum Access Time (ns)	Maximum Operating Current (mA)
CY7C179-8JC, <i>Note (1)</i>	32 K × 18 K	8.5	225
CY7C179-10JC	32 K × 18 K	10.5	210
CY7C1032-8JC	64 K × 18 K	8.5	280
CY7C1032-10JC	64 K × 18 K	10.5	280

Table 8. Configuration Options

Configuration	EPC1	BitBlaster or ByteBlaster Cable	Description
Configuration EPROM, <i>Note (1)</i>	Mounted	Disconnected	To configure the EPF10K30 device with a serial Configuration EPROM, disconnect the BitBlaster or ByteBlaster download cable and mount the programmed EPC1 device in the socket.
BitBlaster or ByteBlaster cable	Removed	Connected	To configure the EPF10K30 in-circuit via the standard parallel port using the MAX+PLUS® II software, remove the EPC1 device, and connect the BitBlaster or ByteBlaster download cable.

Notes to tables:

- (1) This configuration is the default board setting.
- (2) By default, the clock device is not mounted. Users can select a pin-compatible clock device of a different frequency.

References

Refer to the following Altera documents for more information:

- [PCI Master/Target MegaCore Function with DMA Data Sheet](#)
- [Application Note 59 \(Configuring FLEX 10K Devices\)](#)
- [Application Note 86 \(Implementing the pci_a Master/Target in FLEX 10K devices\)](#)
- [FLEX 10K Embedded Programmable Logic Family Data Sheet](#)
- [ByteBlaster Parallel Port Download Cable Data Sheet](#)
- [BitBlaster Serial Download Cable Data Sheet](#)
- [Configuration EPROMs for FLEX Devices Data Sheet](#)

Other references include:

- PCI-SIG. *PCI Local Bus Specification, Revision 2.1*, Portland, Oregon: PCI Special Interest Group, June 1995.
- Brooktree Corporation. *Brooktree Graphics and Imaging Product Databook*. San Diego, California: Brooktree Corporation, 1990.
- Cypress Semiconductor. *Cypress Data Book*. San Jose, California: Cypress Semiconductor Corporation, May 1995.



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